Dot matrix LCD Module Manual

YBC12834

LCD MODULE USER MANUAL

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1. FUNCTIONS & FEATURES

Features

- Dot Matrix: 128×34 Dots
- LCD Mode: FSTN/POSITIVE
- Controller IC:ST7567
- Driving Method: 1/49 Duty; 1/8 Bias
- Viewing Angie: 6 O'clock direction
- 4-Line SPI interface
- Operating voltage: 3.3V
- Operating Temperature Range: -20 to +70℃;
- Storage Temperature Range : -30 to +80℃;

2. MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	57.0L×25. 0W×4.61H	mm
View Area	51.6×15.6	mm
Effective Area	128×34	dot
Dot Size	0.33×0.38	mm
Dot Pitch	0.35×0.40	mm

3. EXTERNAL DIMENSIONS

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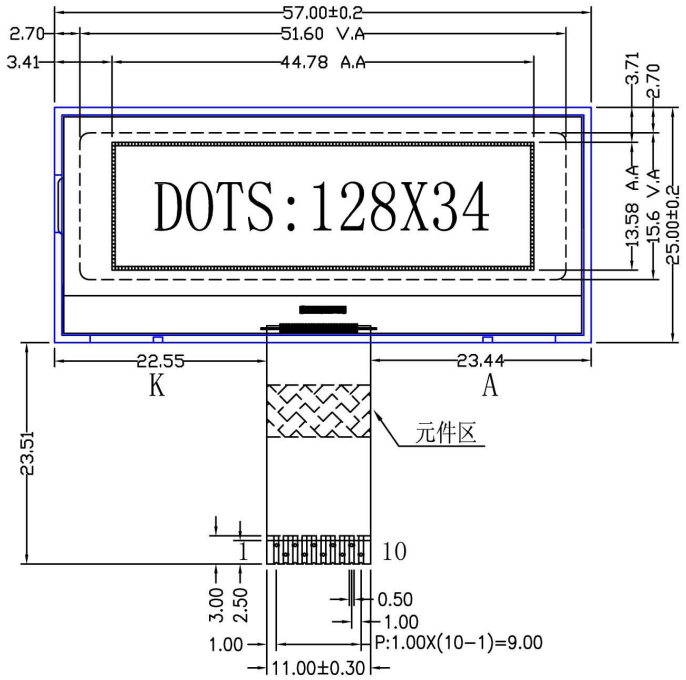
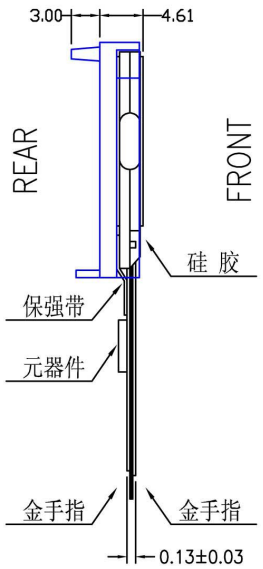
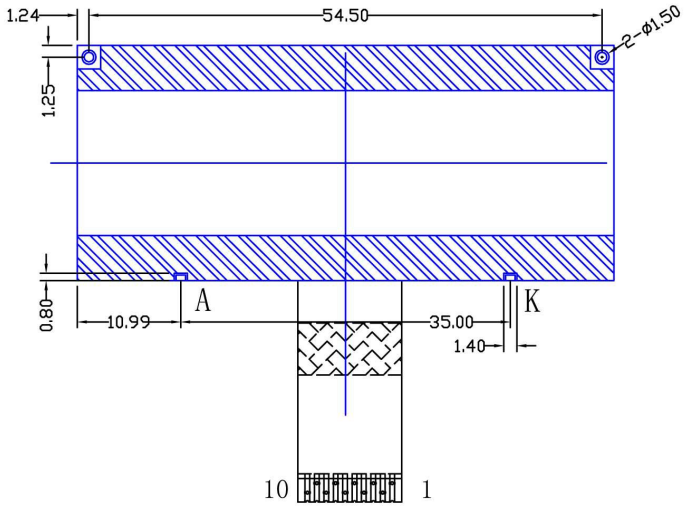
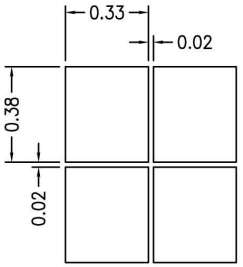
SHENZHEN YABIN ELECTRONICS CO.,LTD

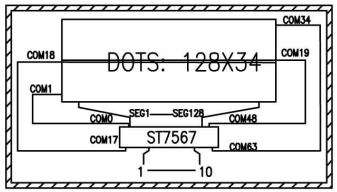




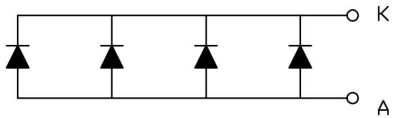




LOGIC ROUTING:



LED Backlight:
(3.0V,60MA)



DISPLAY TYPE: FSTN/POSITIVE
POLARIZER: TRANSFLECTIVE
VIEWING DIRECTION: 6:00-CLOCK
DRIVE METHOD: 1/49DUTY,1/8BIAS
LCD OPERATING VOLTAGE: 6.0v
LCM OPERATING VOLTAGE: 3.0v
OPERATING TEMP: -20 TO 70 Deg.C
STORAGE TEMP: -30 TO 80 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20

深圳市亚斌电子有限公司			CD
		UNIT: MM	SIZE: A4
		SHEET: 1 OF 1	
LCM NO.: YBC12834ZA+LED	DWG NO.: YBC12834ZA+LED		REV: A0
DRAWN BY :	CHECKED BY :	APPROVED BY :	

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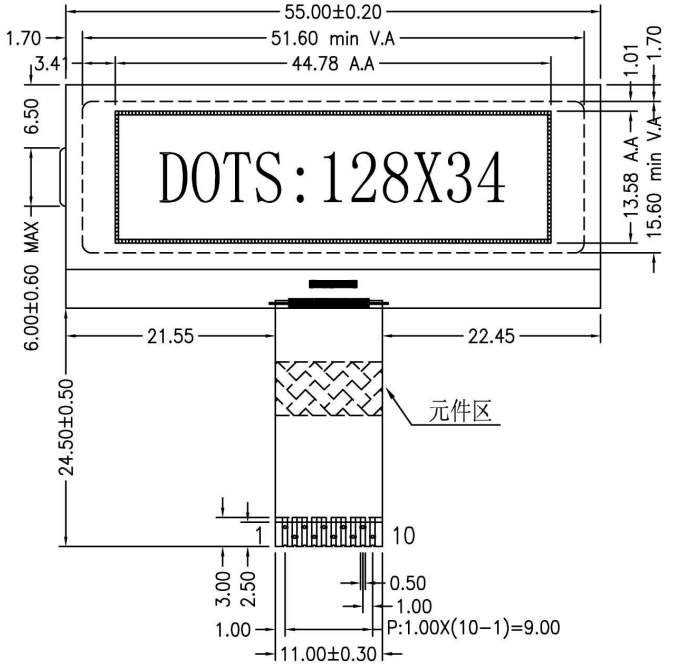

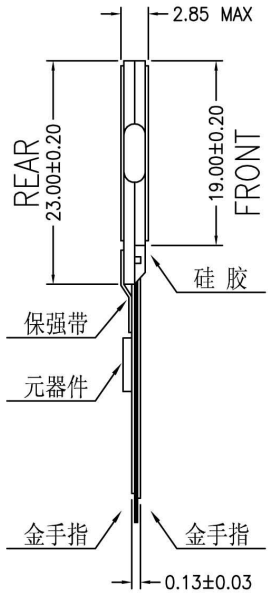

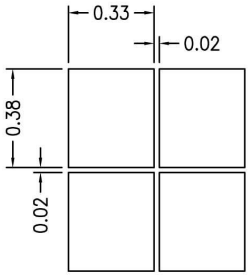

NO	1	2	3	4	5	6	7	8	9	10
PIN	VG	XV0	V0	VSS	VDD	SDA	SCL	A0	RSTB	CSB

DISPLAY TYPE: FSTN/POSITIVE
POLARIZER: TRANSFLECTIVE
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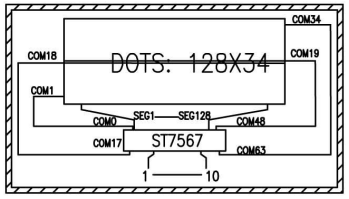
LCM OPERATING VOLTAGE: 3.0v
OPERATING TEMP: -20 TO 70 Deg.C
STORAGE TEMP: -30 TO 80 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20

LOGIC ROUTING:



深圳市亚斌电子有限公司		CD
	UNIT: MM	SIZE: A4
	SHEET: 1 OF 1	
LCM NO.: YBC12834ZA	DWG NO.: YBC12834ZA	REV: A0
DRAWN BY :	CHECKED BY :	APPROVED BY :

4. PIN DESCRIPTION

ITEM	SYMBOL	LEVEL	FUNCTION
1	VG	--	LCD driving voltage (-0.3~3.6V)
2	XV0	--	LCD driving voltage (V0-XV0= -0.3~16V)
3	V0	--	LCD driving voltage
4	VSS	0V	Power Ground
5	VDD	3.3V	Power Supply For Logic
6	SDA	H/L	Serial data input
7	SCL	H/L	Serial clock input
8	A0	H/L	It determines whether the access is related to data or command. RS="H" : Indicates that signals on DB[7:0] are display data. RS="L" : Indicates that signals on DB[7:0] are command.
9	RSTB	H/L	Hardware reset input pin. When RST is "L", internal initialization is executed and the internal registers will be initialized.
10	CSB	H/L	Chip select input pin. Interface access is enabled when CSB is "L". When CSB is non-active (CSB="H")

5. MAXIMUM ABSOLUTE LIMIT (T=25°C)

Items	**Symbol**	**Min**	**Max**	**Unit**	**Condition**
Supply Voltage	Vdd	2.4	3.3	V	Vss=0V
Input Voltage	Vin	0	Vdd	V	Vss=0V
Operating Temperature	Top	-20	+70	℃	No Condensation
Storage Temperature	Tst	-40	+80	℃	No Condensation

Note: Voltage greater than above may damage the module
All voltages are specified relative to Vss=0V

6. ELECTRICAL CHARACTERISTICS

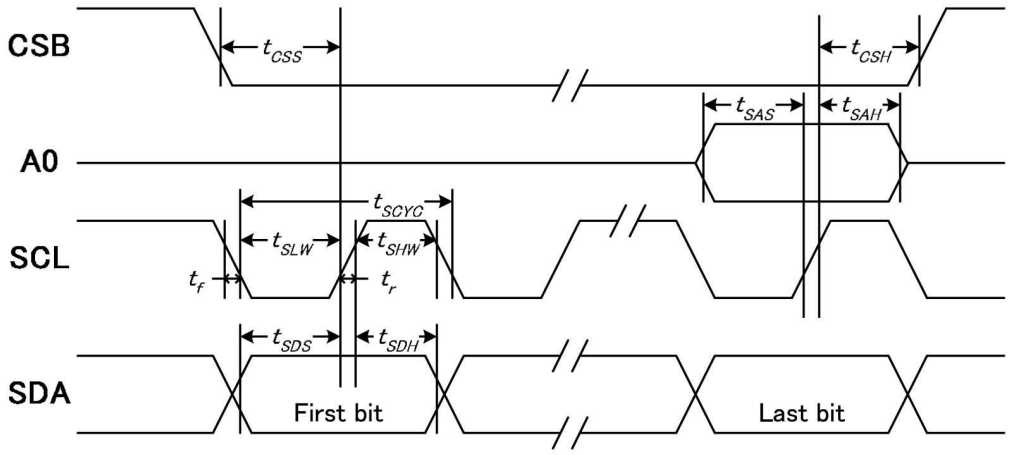
6.1 DC Characteristics (VSS=0V, Ta=-20~+70° C)

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.7	—	3.3	V	VDD1
Operating Voltage (2)	VDD2			2.4	—	3.3	V	VDD2
Operating Voltage (3)	VDD3			2.4	—	3.3	V	VDD3
Input High-level Voltage	V_{IHC}			0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}			VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V		0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V		VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}			-1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}			-3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25°C	Vop=8.5V, ΔV=0.85V	—	0.6	0.8	KΩ	COMx
			VG=1.9V, ΔV=0.19V	—	1.3	1.5	KΩ	SEGx
Frame Frequency	FR	Duty=1/65, Vop=8.5V Ta = 25℃		70	75	80	Hz	

Note:

The Current Consumption is DC characteristics

7. System Bus Timing for 4-Line Serial Interface



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		50	—	ns
SCLK “H” pulse width		tSHW		25	—	
SCLK “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		40	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		100	—	ns
SCLK “H” pulse width		tSHW		50	—	
SCLK “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		60	—	

(VDD1 = 1.8V , Ta =25°C)

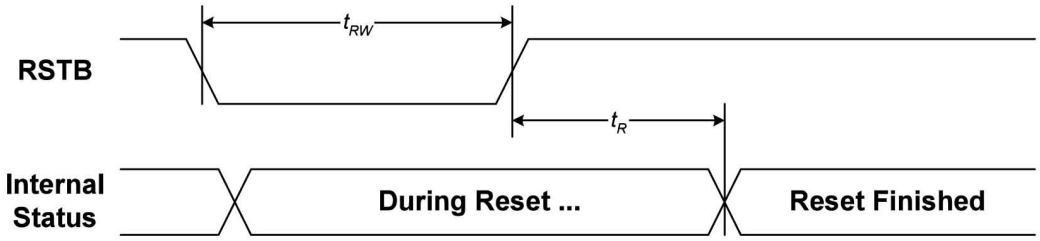
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		200	—	ns
SCLK “H” pulse width		tSHW		80	—	
SCLK “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

8. Hardware Reset Timing

Hardware Reset Timing



(VDD1 = 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset “L” pulse width	tRW		1.0	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0	—	

(VDD1 = 1.8V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

9. INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4) Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Test	0	0	1	1	1	1	1	1	1	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

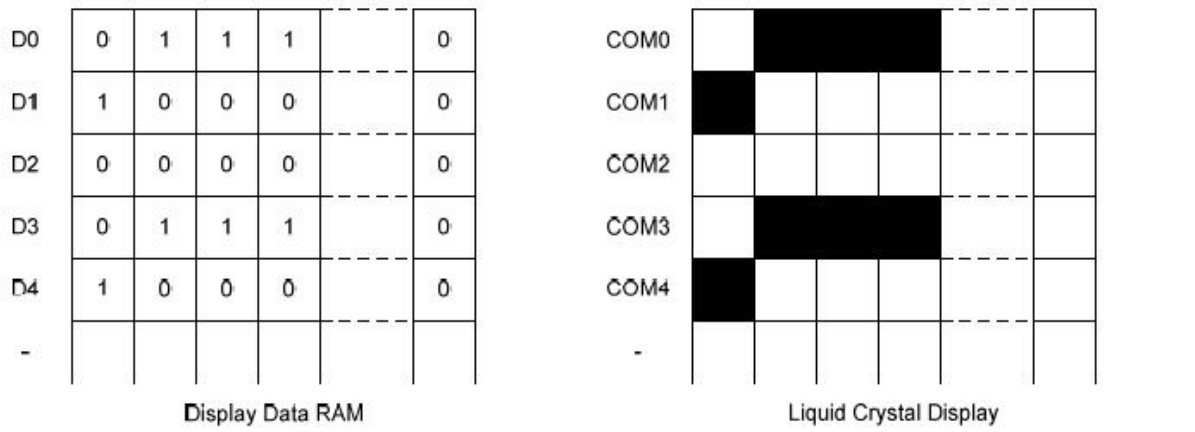
NOTE:

- Do not use any other commands not listed, or the system malfunction may result.
- For the details of rte display commands, please refer to ST7567 datasheet.

10. Display Data RAM (DDRAM)

ST7567 is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column

addresses are specified.
The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0).
The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



Addressing

Data is downloaded into the Display Data RAM matrix in ST7565as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

Page Address Circuit

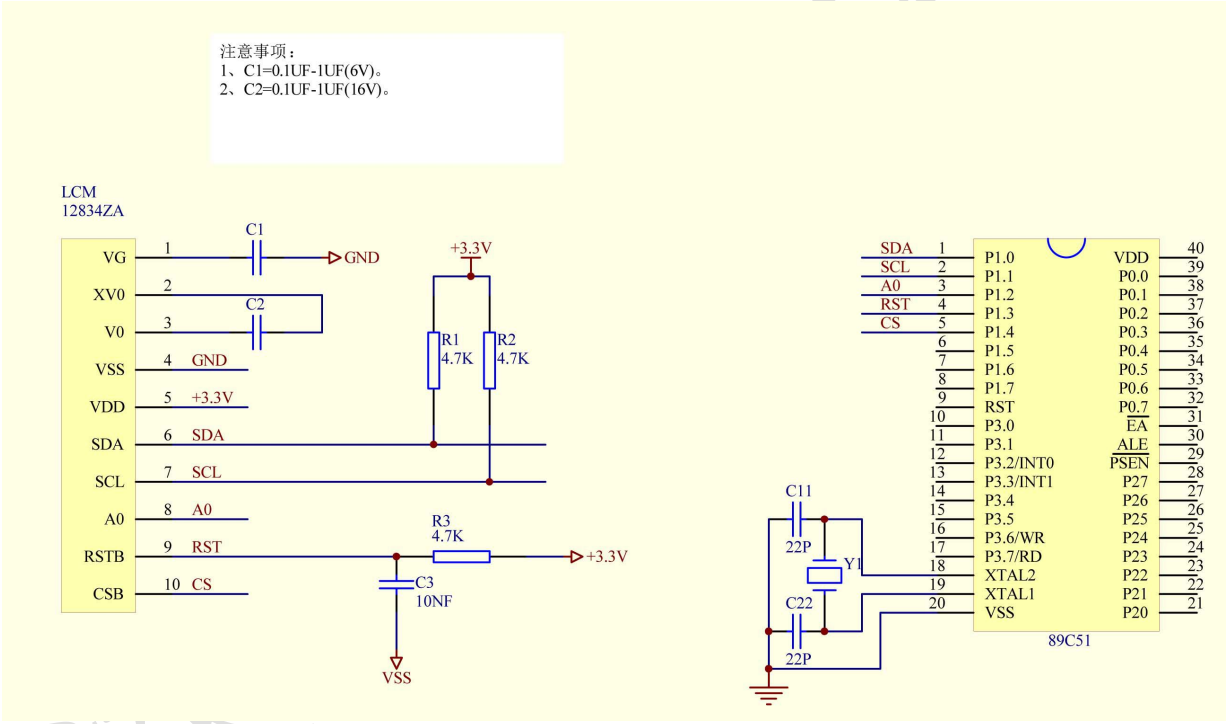
This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons with only one valid bit: D0.

Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”) because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Please refer to ST7567 datasheet.

11. Application Circuits



12 .DESIGN AND HANDING PRECAUTION

12.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module.Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

12.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

12.3 Never attempt to disassemble or rework the LCD module.

12.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
12.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
12.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
12.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
12.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
12.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
12.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12.11 Take care and prevent get hurt by the LCD panel edge.
12.12 Never operate the LCD module exceed the absolute maximum ratings.
12.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
12.14 Never apply signal to the LCD module without power supply.
12.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
12.16 LCD module reliability may be reduced by temperature shock.
12.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module